IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered). Please AMEND claims and ADD new claims, in accordance with the following:

---

1. (CURRENTLY AMENDED) A plasma display driving method wherein:

each frame comprises plural subfields, each of said subfields including a reset period performing an erase discharge to initialize a wall charge distribution in each cell, an address period generating a wall charge distribution in accordance with display data, and a sustain discharge period discharging in accordance with the wall charge distribution generated in the cell during said address period, to emit light; and

said reset period includes first and second erase discharge periods performing erase discharges ~~for cells~~ to erase wall charges accumulated in cells wherein the erase discharge in said second erase discharge period is achieved by applying, to a first electrode, a first erase pulse whose application voltage continuously changes with time in a positive direction and applying, to a second electrode, a second erase pulse whose application voltage continuously changes with time in a negative direction.

C1 cont

2. (PREVIOUSLY AMENDED) A method according to claim 1, wherein:

a full-surface write discharge and a full-surface erase discharge are performed during said reset period only in a specific subfield among the plural subfields in each frame;

erase discharges to erase wall charges accumulated in cells are performed during said reset periods in the remaining subfields without performing said full-surface write discharges; and

the erase discharges performed separately in said first and second erase discharge periods are executed in each subfield except for said specific subfield.

3. (CANCELED)

4. (CURRENTLY AMENDED) A method according to claim 1, wherein pulse widths of said first and second erase pulses have time widths required to reach ultimate voltages of

said first and second erase pulses.

5. (PREVIOUSLY AMENDED) A method according to claim 1, wherein said first and second erase pulses have waveforms whose change rates, per unit time of the application voltage, change with time.

6. (PREVIOUSLY AMENDED) A method according to claim 1, wherein said first and second erase pulses have waveforms whose change rates, per unit time of the application voltage are constant.

7. (PREVIOUSLY AMENDED) A method according to claim 1, wherein a potential difference, between the respective ultimate voltages of said first and second erase pulses, is approximately the same as a discharge start voltage, between said first and second electrodes, and is smaller than said discharge start voltage.

C1 cont

8. (ORIGINAL) A method according to claim 7, wherein at least one of said ultimate voltages of said first and second erase pulses is variable.

9. (CURRENTLY AMENDED) A method according to claim ~~3~~ 1, wherein the rise start timing of said first erase pulse is synchronized with, or delayed from, the fall start timing of said second erase pulse.

10. (CURRENTLY AMENDED) A plasma display driving apparatus driving a plasma display panel wherein, in each of plural subfields constituting one frame, each of said subfields includes a reset period performing an erase discharge to initialize a wall charge distribution in each cell, an address period generating a wall charge distribution in accordance with display data, and a sustain discharge period discharging each cell in accordance with the wall charge distribution generated in the cell during said address period, to emit light, said apparatus comprising:

a controller performing erase discharges for cells in first and second erase discharge periods in said reset period;

wherein said controller performs the erase discharge in said second erase discharge period to erase wall charges accumulated in cells by applying, to a first electrode, a first erase

pulse whose application voltage continuously changes with time in a positive direction and applying, to a second electrode, a second erase pulse whose application voltage continuously changes with time in a negative direction.

11. (PREVIOUSLY AMENDED) An apparatus according to claim 10, wherein:

said controller performs a full-surface write discharge and a full-surface erase discharges during said reset period only in a specific subfield among the plural subfields in each frame, erase discharges to erase wall charges accumulated in cells during said reset periods in the remaining subfields without performing said full-surface write discharges, and executes the erase discharges, performed separately in said first and second erase discharge periods in each subfield except for said specific subfield.

12. (CANCELED)

C1 Cont

13. (PREVIOUSLY AMENDED) An apparatus according to claim 10, wherein said controller applies, as said first and second erase pulses, pulse voltages having waveforms whose change rates, per unit time of the application voltage, change with time.

14. (PREVIOUSLY AMENDED) An apparatus according to claim 10, further comprising a voltage setting unit setting a potential difference, between the respective ultimate voltages of said first and second erase pulses, to be approximately the same as a discharge start voltage, between said first and second electrodes, and to be smaller than said discharge start voltage.

15. (PREVIOUSLY AMENDED) An apparatus according, to claim 14, wherein said voltage setting unit selectively changes at least one of the respective ultimate voltages of said first and second erase pulses.

16. (PREVIOUSLY AMENDED) An apparatus according to claim 15, wherein said voltage setting unit comprises a first resistor in a pulse generation circuit generating said first erase pulse and a second resistor in a pulse generation circuit generating said second erase pulse, and at least one of said first and second resistors is variable:

17. (PREVIOUSLY AMENDED) An apparatus according to claim 16, wherein said first and second resistors have respective, different resistance values.

C1 cont

18. (PREVIOUSLY AMENDED) An apparatus according to claim 10, wherein said controller synchronizes or delays a rise start timing of said first erase pulse with, or from, a fall start timing of said second erase pulse.